AUTOMATED TEST EQUIPMENT

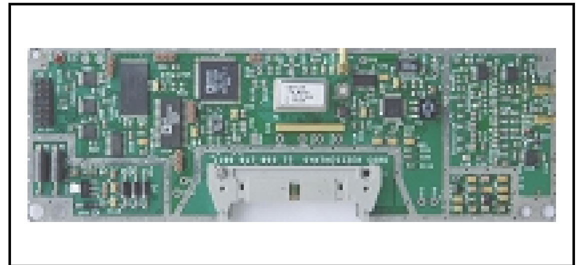
QT2256-320PXI

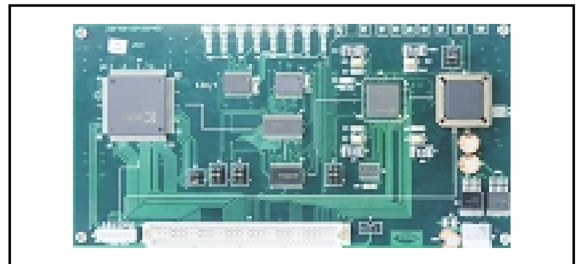
COMBINATION BOARD TESTER

Conventional & New Generation ATEs

- In the past, PCBs (Printed Circuit Boards) had been designed with simple SSI / MSI / LSI and discrete off the shelf standard components and used through hole DIP packages that can be easily tested using a Conventional Board Test ATE either through a card edge functional test or ICT with a bed of nail test fixture or even Clip on test of each device.
- The PCB technology over the years has changed a lot in terms of package density and Functional complexity. The new technology PCBs uses Programmable Logic Devices (PLDs), Field Programmable Gate Arrays (FPGAs), Digital Signal Processors (DSPs) and single chip micro controllers. Often many of the devices are proprietary and with little information on the functionality of the devices. Ball Grid Array (BGA) packages make it more difficult to access the device pins.
- These PCBs are a great challenge to test and diagnose faults down to component level using a conventional ATE system. The reasons are quite obvious, the device package density and the use of FPGA / CPLD / DSP devices in place of standard devices.

A conventional PCB

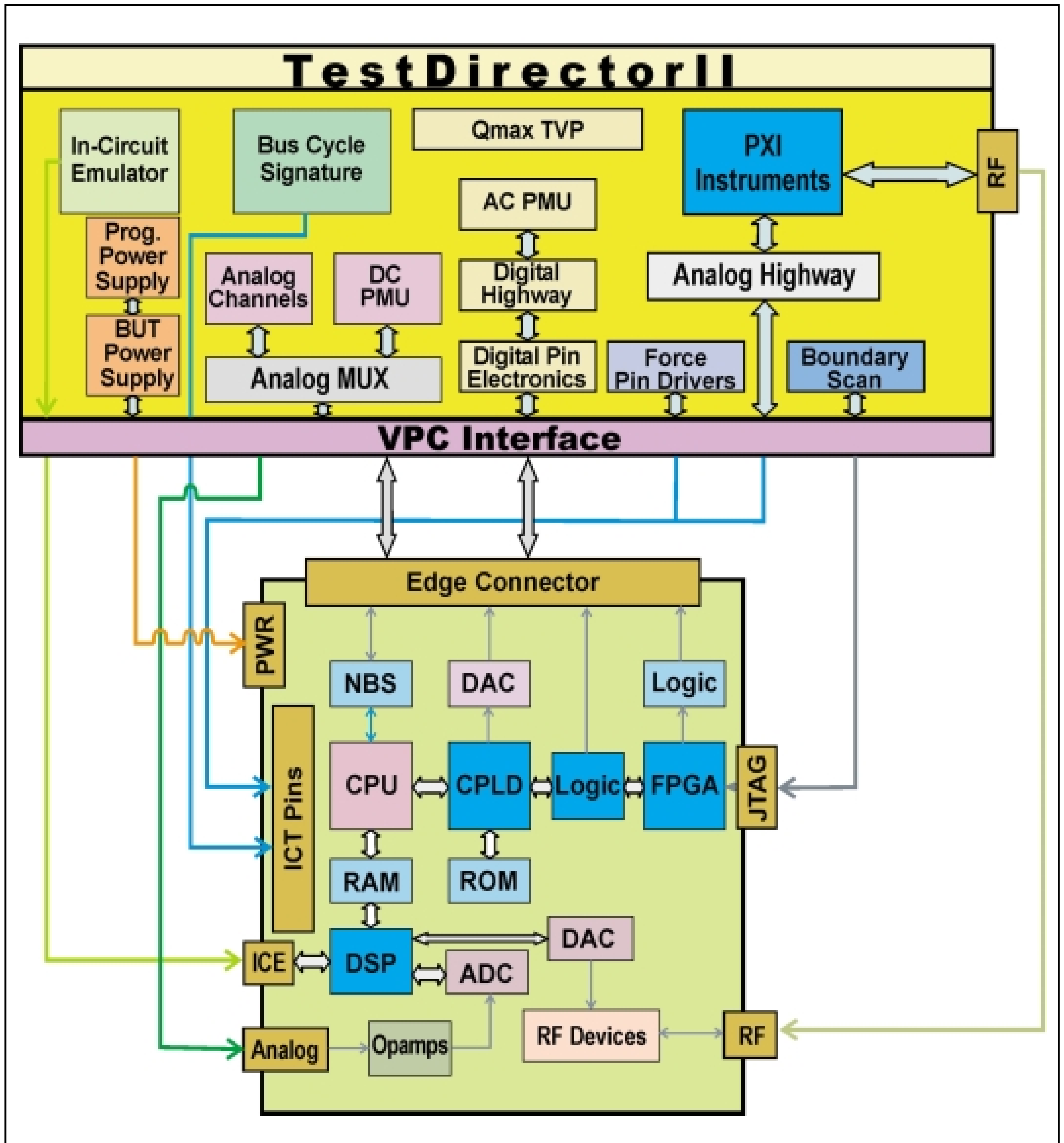




Some new generation PCBs

- In case of Manufacturing test, an expensive bed of nail test fixture (Due to high density of test pins) and a MDA (Manufacturing Defect Analyzer) type of tester can detect faults such as open / short, wrong value components, missing components, wrong orientation etc and can do some cluster level functional test.
- But in maintenance of such PCBs, one will seldom find such manufacturing defects as the PCB was functional before it failed and the most probable faults are a component failure. In such cases, a MDA can not help and one will require a functional tester.
- Testing such new technology boards functionally are not an easy job and require altogether a new generation ATE system with multiple test techniques and advanced test software.
- As the PCB technology advanced, so is the test technology. A good example is the IEEE standard 1149.1 Boundary Scan Test (BS Test), which allows toggling of a device pin through a simple serial interface (JTAG) thus making every I/O pin of the device as a virtual test point. This is a solution for high pin count mega chips.
- A stand alone BS Test will not suffice, as one will require a synchronized card edge test (Driven / Sensed by an ATE pin driver) along with BS test to cover faults on the glue logic devices between BS Devices and the edge connector.
- Please note that all the devices are not BS featured and certain DSP devices need ICE (In-Circuit Emulator) to toggle the device pins and thereby execute a functional test covering RAM / ROM and logic around the DSP device.
- Testing and detecting faults on a CPU or micro controller based board is often a challenge for Test Program Set (TPS) developers on a conventional ATE as it requires expensive CPU models and expertise.
- Qmax's Patented Bus Cycle Signature System, offers simple learn and compare technique of digital bus cycle signatures, without having to invest huge money and time in developing test vectors for TPS.
- It is often experienced by ATE Managers, Board that Passes the functional test in the ATE Lab, fails to work reliably in the field and returned as field return. This creates additional unscheduled work load and also the credibility and reliability of the ATE Lab becomes a question.
- Most commercial ATEs does only functional test and do not carry out DC / AC parametric test, which are very essential in increasing the fault coverage and for achieving near zero field returns.

Overview of Qmax's New Generation Board Test ATE System:

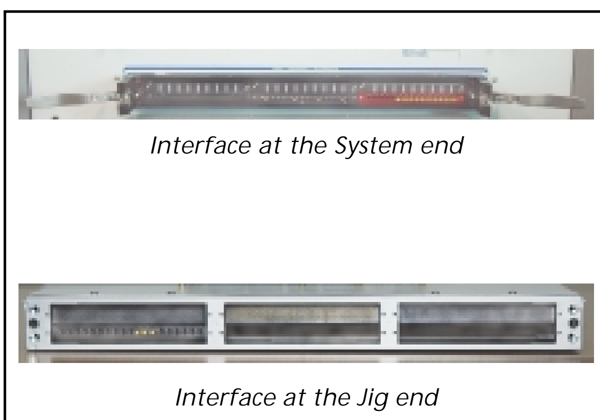


Qmax QT2256-320PXI ATE system, the best solution for ATE Labs:

- ATE QT2256-320PXI system is designed as a Combination Board Tester capable of testing highly complex and dense PCBs employing various test techniques on a single platform.
- It can perform **Board Level Functional Test through edge connectors of a PCB, and guided probe diagnostics** utility to reliably repair Digital/Analog and Mixed Signal PCBs of various complexities for conventional PCBs.
- It is an In-Circuit Device / cluster tester when **High Current Pin Driver** options are installed and interfaced to the UUT either through clips / probes or nail bed. Standard configuration is 64 Channels high current Pin Drivers.
- It has in-built 20MHz 12bit Analog Driver / sensors synchronized with digital drivers for covering analog / mixed signal devices.
- Integrated **Boundary Scan Test** controller (Up to 4 Chains) and software package can be used to test today's PCBs with high density / high pin count devices. Uses latest technology Boundary Scan hardware with RAM based drivers / sensors in synchronization with ATE digital and analog pin drivers.
- To effectively test CPU based boards without excluding the CPU from the test, the system offers optional Qmax patented **Bus Cycle Signature System**.
- In-Circuit Emulator Support for testing DSP based Board Function.
- **Parametric Measurement Units (PMU)** enables testing of the DC parametric of device pins on the edge connector for input bias current, Fan out capacity and Tri-state leakage currents to further enhance fault coverage and avoid unwanted field returns.

A General Purpose Test Jig

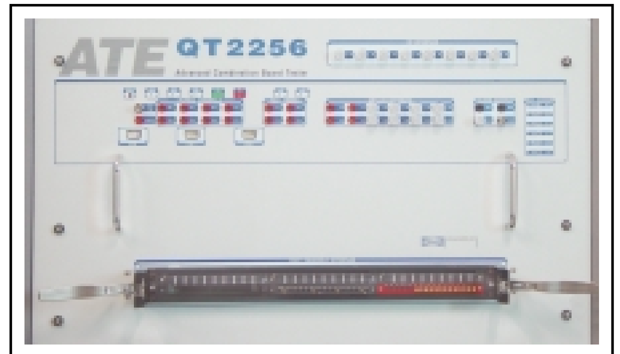
VPC Test Channels Interface



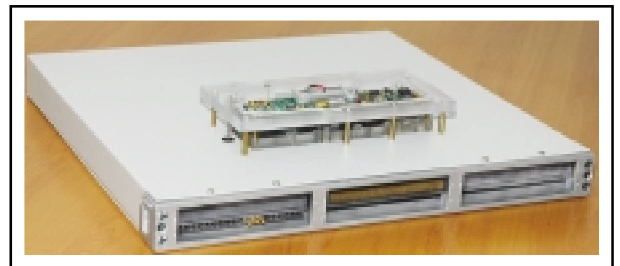
Interface at the System end

Interface at the Jig end

Programmable Power Supply



ATE Front Panel view

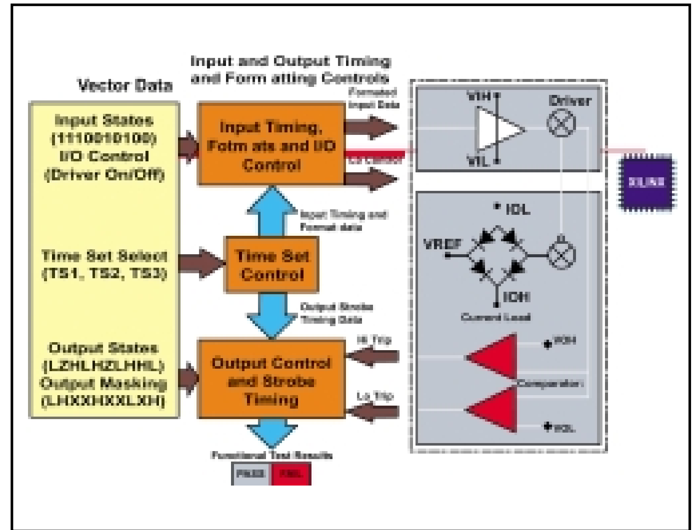


A Test Jig with VPC Interface

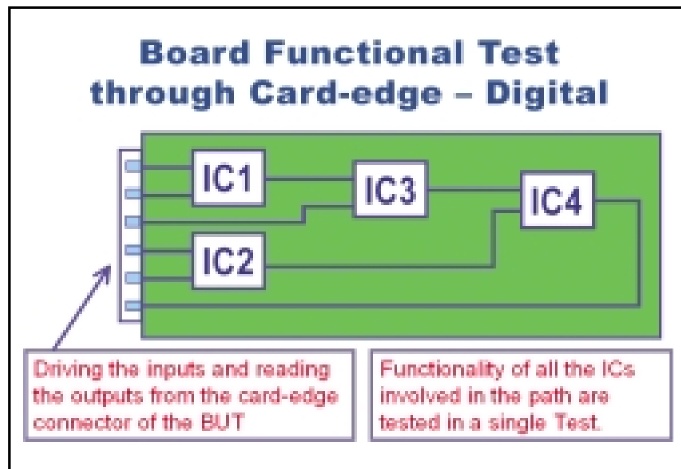
- Optional **AC Parametric Tests** for propagation delay, rise / fall time and pulse width measurements.
- The capabilities can be further enhanced with optional IEEE instrumentation or **PXI based Instrumentation** and control through TestDirector II software.
- Analog Highways and relay matrix modules are used in routing the test pin to external measurement IEEE or PXI Instruments of user choice.
- Uses Virginia Panel Test adapter Interface for highly reliable Unit Under Test (UUT) Interface Panel provides up to 384 signals, 19 power (50A each) and 19 RF connectors.
- The ATE is interfaced to an external Host PC using a 32 bit, 33MHz PCI interface card allowing a maximum data transfer rate of 132 Mega bytes per second.
- It is a modular design with upgrade options. The basic system comes with 64 High Current Digital Channels, 64 digital channels with 50 Ohms source impedance, 8 Flying channels 2 Analog channels and 5 fixed UUT power supplies. It can be easily upgraded to 320 or more Digital Channels, 4 Analog Channels and with Programmable UUT power supplies, IEEE or PXI External Instrumentation, Bus Cycle Signature System, ICE and Integrated Boundary Scan Test.

State-of-the-art technology

The heart of the test system is a FPGA based highly programmable dedicated test vector processor with Digital Clock Management System. It has 4k x 60 bit RAM for Instruction Register and Test Sequencing. Up to 4096 test sequences can be pre-programmed to run automatically with options for conditional branching. This Test vector processor controls the timing and construction of Drive waveforms that will be driven into the UUT and to acquire response data. Data formatting capability for NR, RO, RZ, ZD and SBC are supported. All digital channels have 1MB X 8 RAM. All analog channels have 1MB X 24 RAM. The Four Analog Channels can be multiplexed to any of the 320 channels and 8 flying channels. The basic timing unit is programmable from 10 ns to 655us in steps of 10ns. A Test Cycle with 4 basic timing units results in 40ns data rate or 25MHz test rate. Digital highways provide for synchronization of the test cycle to UUT events and digital timing measurements through tester pins.



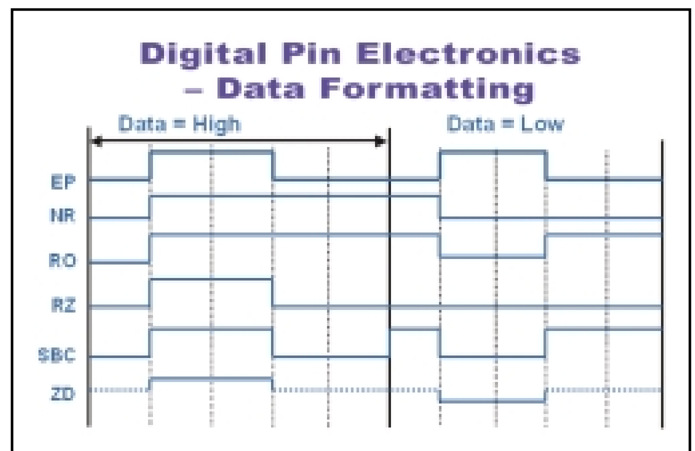
Digital Pin Electronics



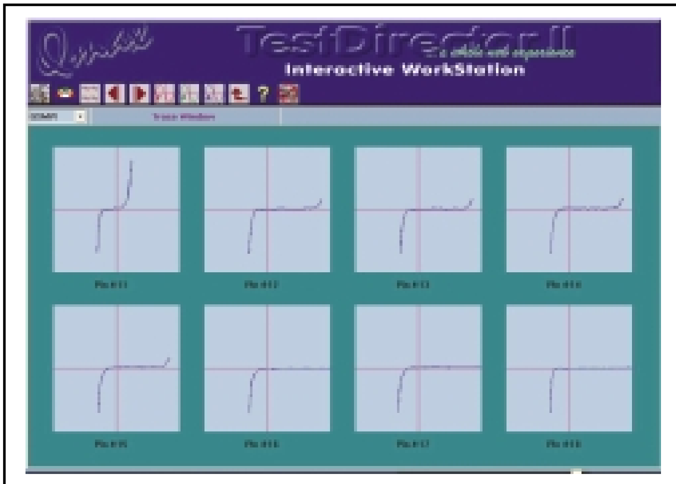
There are multiple options for Digital Pin Drivers. These include High speed 50 Ohms type and High current Back Driving type Pin Drivers. The Drive and threshold levels are programmable. System supports two pallets of Drive and Threshold Level within +/–10V and in resolutions of 5 milli volts. High Current Back Driving Pin Drivers can select its levels from either of the 2 preprogrammed pallets. The Standard 50 Ohms Pin Drivers can be individually programmed for its own drive / sense levels. Optionally one can include a programmable Current Source / Sink up to 35mA of load current for each Digital Channel to load output pins and test. The current load can be turned-on or off on the fly.

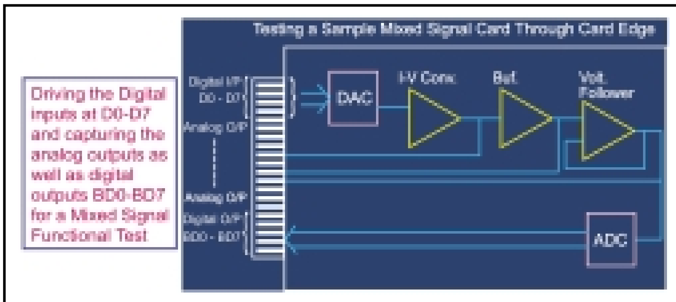
Programmable Timing Generator / Pin Data Formatter

Basic Timing Unit in QT2256-320PXI is programmable from 10ns to 655µS. A Test Cycle or Event Frame can be from 4 basic timing units (40ns-min) to 255 timing units. Up to eight Test Cycles can be pre-programmed. Each of the Test Cycle can have up to eight event pulses preprogrammed. QT2256-320PXI supports NR (Non Return), RZ (Return to Zero), RO (Return to One), SBC (Surround by compliment) and ZD (Return to Z state) data formats. This feature allows the Drive phase and Test Window to be placed within a Test cycle using one of the 8 pre-programmed Event Pulses EP0 to EP7.



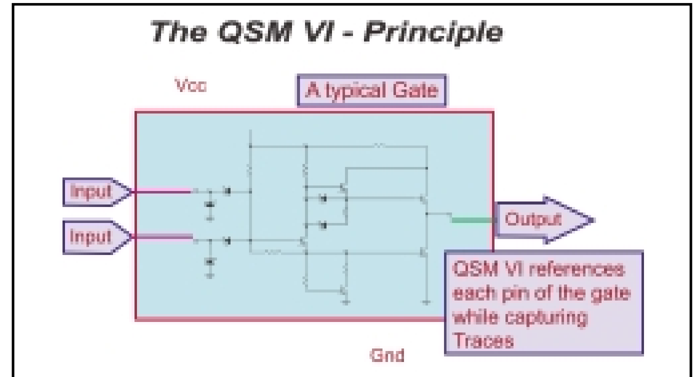
Analog Sub-System





The Analog Subsystem has maximum of Four Channels with 12 bit accuracy and 20MHz sampling rate. These four programmable analog channels can be used as stimulus / response channels and are fully synchronized with the digital channels. They can be used as Analog input / output channels within a voltage range of +/– 13V with current capacity of up to +/– 260mA for testing analog and mixed signal portion of the PCBs under test.

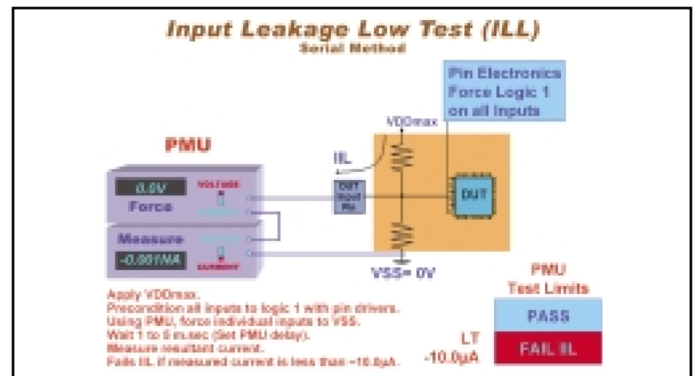
Using two of these analog channels, QSM VI test is carried out for any pin to any pin combination. This QSM VI Learn and compare technique can be used for these devices, where no data sheet is available, no ICE, no Boundary Scan. This test technique is quite effective in repair.

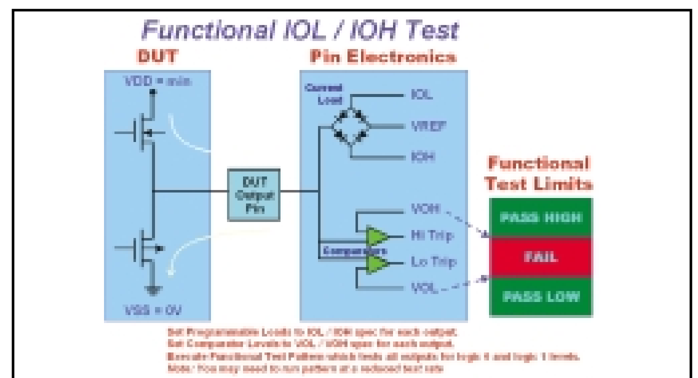


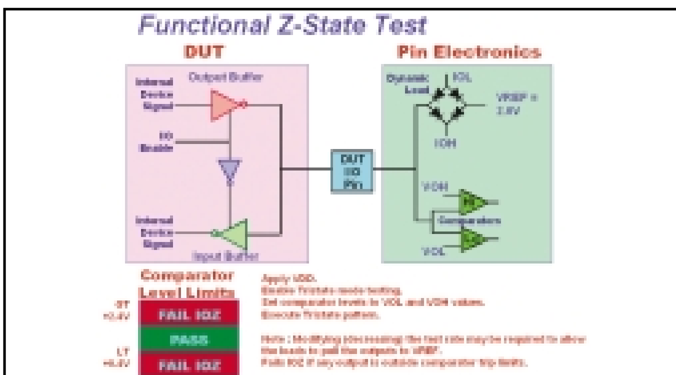
Enhanced Fault Coverage

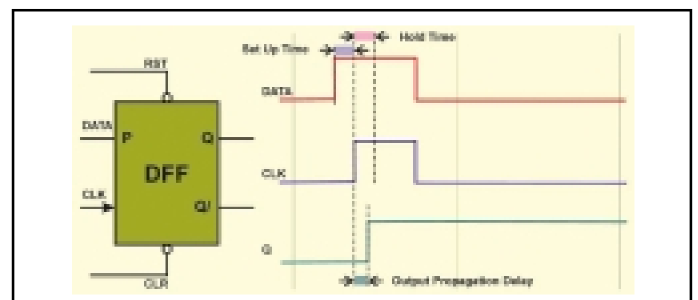
They can also be used as DC Parametric Measurement Units (PMUs) that are normally found only in High-end Semi-con test systems. In PMU mode they can Force Voltage and Measure Current (FVMC) or Force Current and Measure Voltage (FCMV). FVMC is used to measure Input Bias Currents of Digital Input pins on the Unit Under Test to compliment the Functional test and ensure the Input Bias Currents are within specification and the Digital Inputs are not over loading their input signals. ATE pin drivers drive up to 50mA or more and thus will be able to drive a faulty input pin that overdraws current and may pass the functional tests. This undetected fault may cause a problem when the PCB is fitted back into the equipment. Conventional ATE does not test this parameter. QT2256-320PXI has higher fault coverage because of this important feature. Similarly, Tri-State output leakage currents can be tested in QT2256-320PXI apart from the functional test. A leaky tri-state pin may cause problem when the board is fitted back in its original equipment. AC parametric measurements help detect timing faults.

Optional AC Parametric Measurements can help measure Set up / Hold times, propagation delay, rise and fall time to ensure reliable operation of the unit under test.

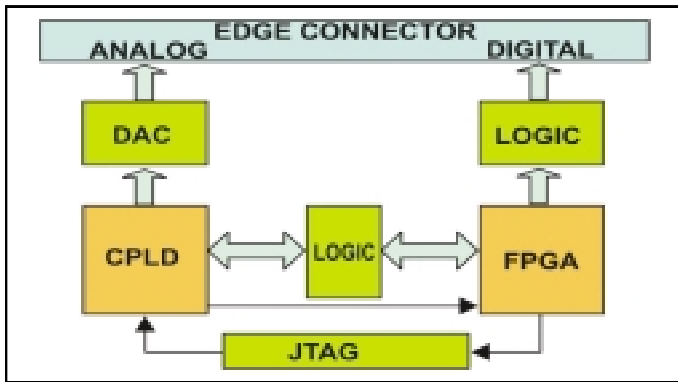








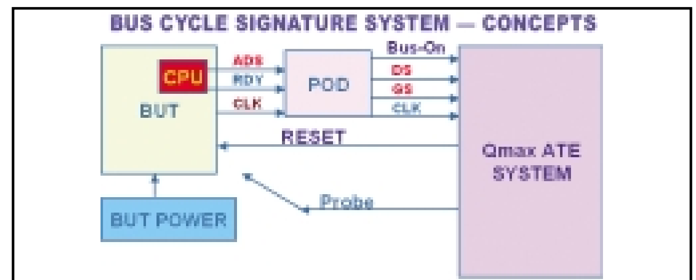
Fully Integrated Boundary Scan *(Optional)*



This involves testing of Boundary Scan devices using the Test Access Port (TAP) controller (TDI, TDO, TMS, TCK and TRST — Optional), provided in the device. Boundary Scan feature is available in Qmax ATE compliant with IEEE standards 1149.1 for all JTAG formats. All 320 digital channels can also be used in setting up logic levels at the card edge / test pins of the board under test, while executing boundary scan test and thus enabling complete test of the board under test for integrity, functional test for both BS and non BS devices using the Qmax's exclusive waveform editor including analog for visual test pattern generation and comparison. System support more than one JTAG chain to accommodate BS chains with different voltage levels such as 2.5V, 3.3V or 5V

Signature Analysis *(Optional)*

In Qmax ATE – QT2256-320PXI, every channel is capable of acquiring logic sates of each digital pin at specified timing strobes. The resultant bit stream is compressed into a 32bit Signature word and thereby building a unique signature for each test channel. Qmax has U.S and U.K. Patent rights for their advanced Bus Cycle Signature System to test CPU based boards running on its own clock speed. Each type of CPU will require an external POD to adapt to the test system.



In-Circuit Emulator Option for DSP devices:

There are many popular DSP devices, without Boundary Scan option but with In-Circuit Emulator port. The Emulator port is similar to the serial interface. Using the Emulator, one can toggle the Device pins and can carryout functional test of RAM / ROM and other logic devices around the DSP. This may include even ADC / DAC test. Analog voltage forcing and sensing can be done using the Analog channels of the Qmax ATE system.

TPS Migration from earlier generation ATE Systems:

- Qmax can provide services for migration of TPS developed in legacy ATEs like Schlumberger, GenRad, Fluke etc., into Qmax ATE systems.
- Once converted into QT System, test programs can be further enhanced to increase fault coverage taking advantage of unique test capabilities of QT systems such as the RAM based analog channels and PMU functions.
- IEEE standard 1455 DTIF format supported.

Hardware Features:

- Main test vector processor board with fully programmable timing generator supports Factron's S720 /790's Standard and Precision timing generator as well as other Legacy ATE systems such as Fluke and GenRad.
- RAM resident programmable event frames and event pulse specification.
- Data format capability for Non Return, Return to Zero, Return to one, Return to z and Surround by compliment.
- Digital subsystem with 1M x 4 bits drive RAM, 1M x 2 bits acquisition RAM and 1M x 2 bits compare RAM.
- Internal 100MHz clock or external clock input (100KHz to 50MHz Max) with phase lock loop and advanced digital clock management.
- External event synchronization for up to 320 test pins, conditional / unconditional loop iterations of up to 32,000 loops.
- Digital measurement modes – Leading edge, Trailing edge, Dual edge, Window, Glitch and Signature Analysis mode.
- Four Digital highways for routing external clock, frequency measurement, time measurement between two events of UUT pins etc.
- Frequency measurement for up to 100 MHz (Direct input) or up to 50MHz through tester pin.
- Pulse width / Time between events measurement with resolution of 10 ns through test channels.
- 12 X 32 analog highways matrix with 30 MHz bandwidth and relays rated for 115V, 0.5 amp current.

Software Features:

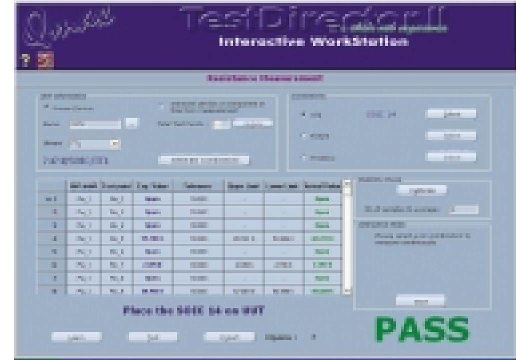
- TestDirector II TPS Development Studio Software for new TPS development and debug.
- *Python*TD is a high level language similar to Mediator with Menu assisted syntax selection and options. When stepped through, it shows the generated graphical test patterns in a Digital / Analog / Mixed signal workbench in another window.
- Graphical Digital / Analog / Mixed signal workbench can also be edited graphically and saved back in Python text.
- Simulator can be invoked and expected logic states for output pins viewed in graphical mode.
- Probe and Compare / Tailor traces facilities.

Qmax QT2256-320PXI Software Platform:

Qmax **TestDirector II** (TD2) software, which runs under Windows XP Professional edition, consists of ***TD2 Interactive WorkStation*** for instant test of a PCB using Qmax's General Purpose Test adapter, ***TD2 TestSequencer*** (TPS Development Studio) for sequencing various tests for a board functional test, optional ***TD2 Integrated Device Development Environment (IDDE)*** for developing new device test programs, ***TD2 TestStation*** for operator Level use of the Test Program Set.

TD2 – Interactive:

These tests can be performed on any PCB instantly using clips / probes along Qmax Device Library and or Learn and compare technique.



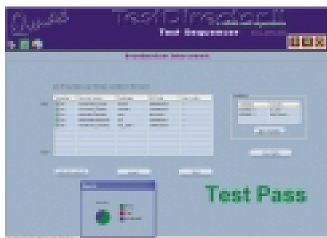
- Out-Circuit Test of Devices
- In-Circuit Test of Devices
- Card Edge Functional Test with Guided Probe Back Tracking.
- Open / Short Test
- RLC Measurements
- Voltage / Frequency measurements
- QSM VI Tests
- Oscilloscope and Function Generator
- Boundary Scan Tests.

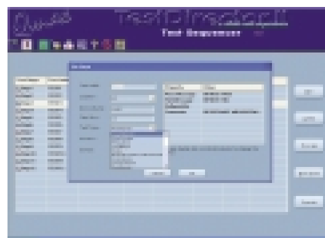
TD2 – TestSequencer (TPS Development Studio):

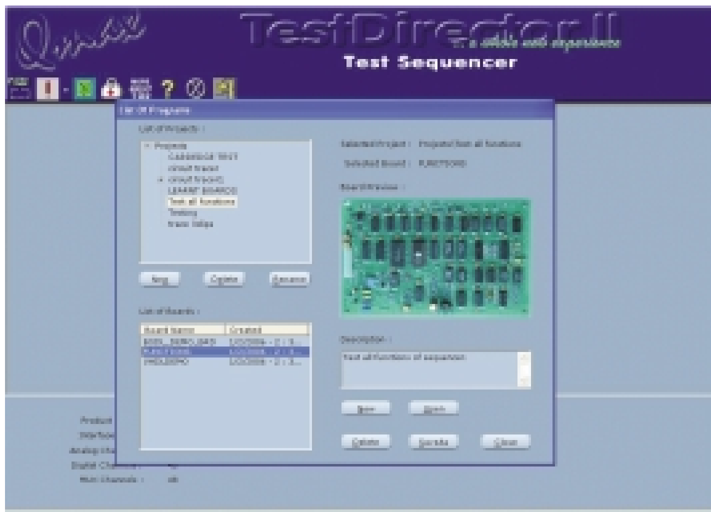
This software package Sequences Test Flow and Guides the user through the entire Test procedure and generates detailed error logs.

For generating Test Program Set for PCB under test.

- Inputs accepted are Bill of Materials, Net-list entry or EDIF import and optionally the Gerber file for PCB layout or PCB image file and Schematic Image file.
- User can generate digital / analog / mixed signal test vector for board initialization and a series of functional test done either graphically or using the Qmax's ***Python*TD** test language.
- The expected output response of the PCB under test can be **Defined** using an expression or **Mark for learning** from known good board for analog / digital and mixed signals or **Simulated** using IEEE standard VHDL simulator for digital signals.
- Features include, Guided Probe Back Tracking, Fault Tree, PCB layout / PCB Image / Schematic image for paperless repair.



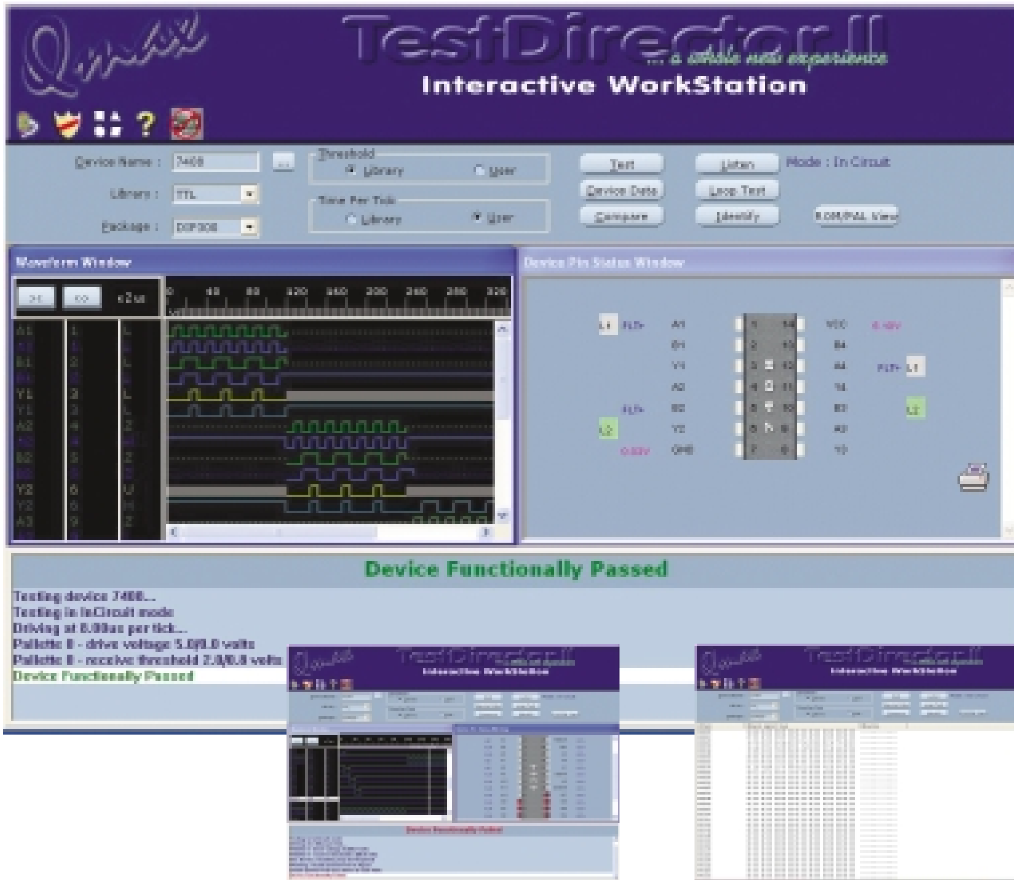




A typical Test Sequence for a board may contain the following tests.

- Open / short test / fixture wiring tests.
- Measurement of RLC, and Diode values.
- QSM VI Tests.
- Board Power supply Measurements, Frequency Measurements.
- Functional Test using Internal or external resources through edge connector / test points.
- Integrated Boundary Scan Test for BS devices such as ID code read, User code read and Interconnect test.
- Testing of Non BS devices and logic devices through JTAG pins of BS devices, edge connector and test points.
- Bus Cycle Signature Test for CPU based boards.
- DC Parametric Test - Input Bias Current / Output Load test / High Impedance check for Tri-state / Bus Devices.
- External Instrument Test Routines for IEEE or PXI.

In-Circuit Functional Test:



Qmax's ICFT / QSM Software Package for In-Circuit test of digital / analog / mixed signal devices including cluster test using 22,000+ Qmax Models.

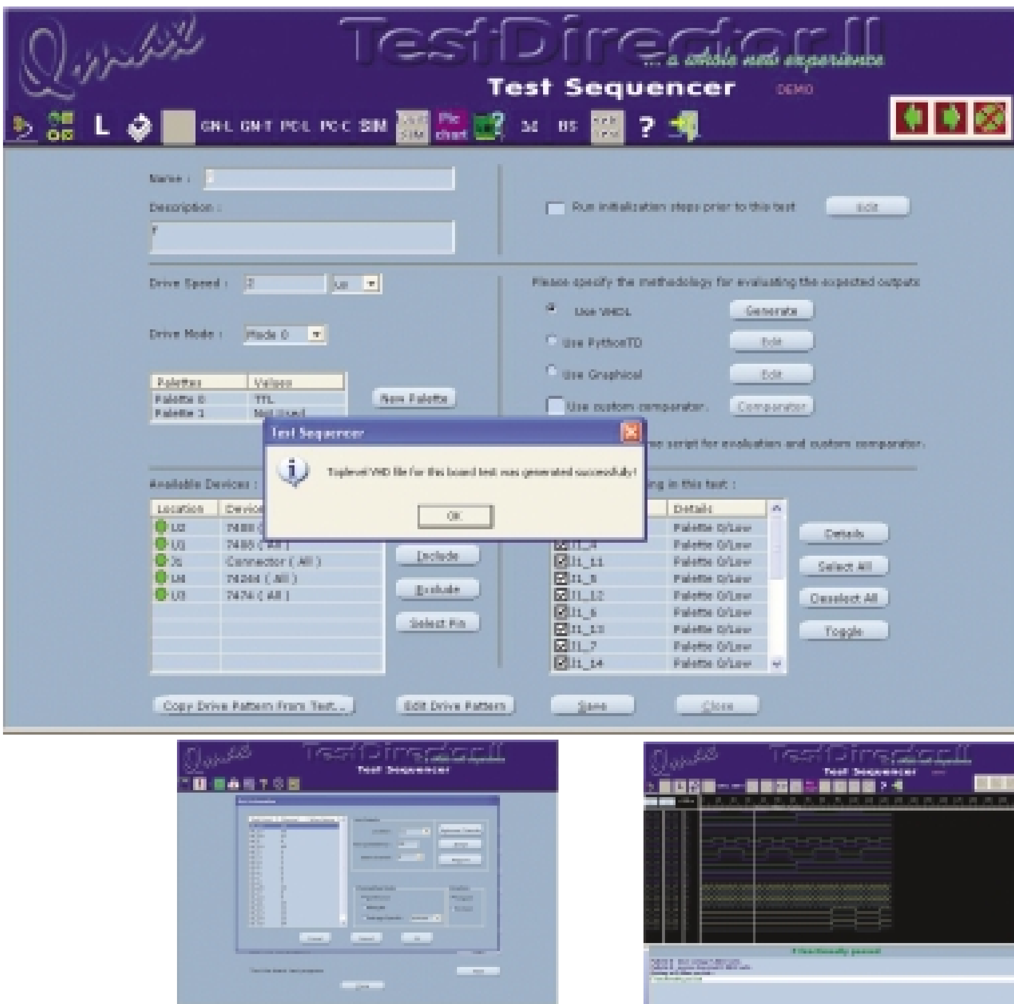
Test can be carried out using Clips / probes or nail bed.

Device links between pins can be either learnt from a known good board for comparison with a suspect board. OR if netlist is available it can be verified.

Automatic Guarding guide is available while testing Bus devices and the system has the ability to trace links between Bus Devices to determine effective guard pins. Optionally this information can also be extracted from net list if available, while testing Bus Devices and OC / OE devices.

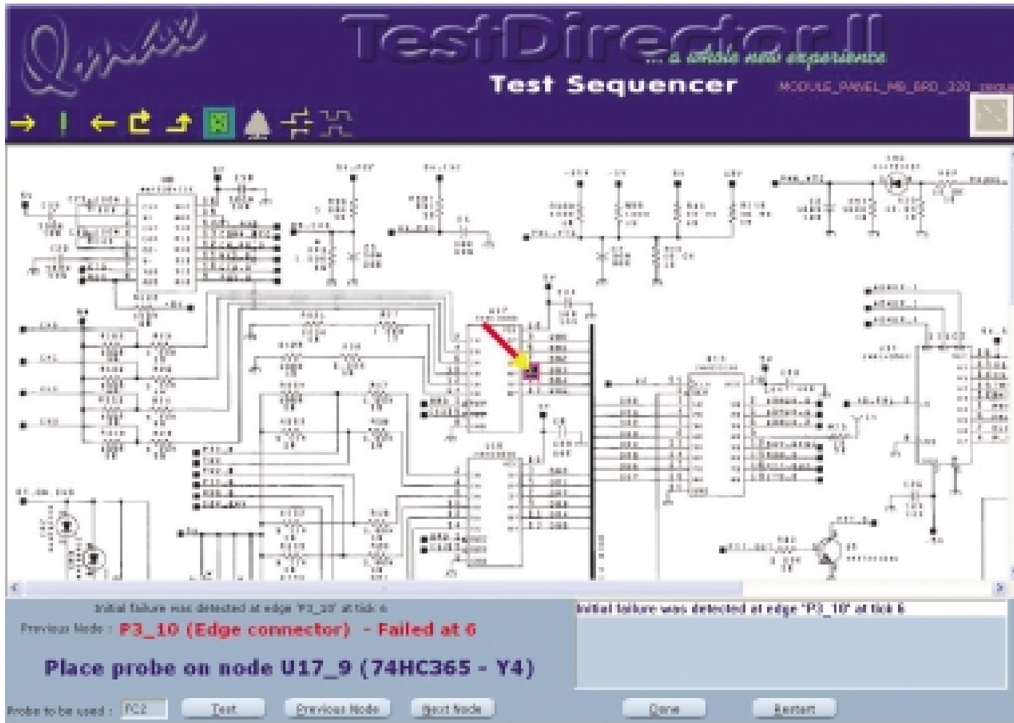
QSM VI Learn / Compare for devices that cannot be modeled and simulated.

Functional Test by Board Level Simulation

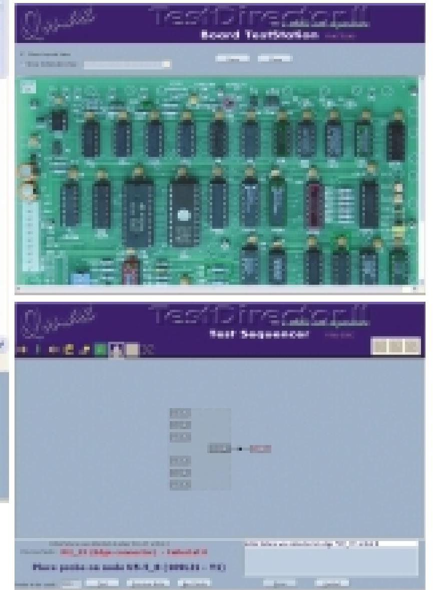


For Board Functional Test and Guided Probe Back Tracking diagnostic software, a simulator is used to predict the output response of the Board and its internal nodes and compared with actual output response in detecting faults and to back track the failure. TD2 supports industry standard simulators both off-line and on-line simulation modes. Off-line simulation does not provide any predicted output unless the board under test has been initialized to home state and thus suffers accurate diagnostics in case the board fails to initialize. This is especially significant if the board under test had many state machines / flip-flops and counters and all of them have to be initialized before any simulation can take place. On-line simulation method is pioneered by Qmax over the years and has proven to be accurate in fault diagnosis even if the board under test fails to initialize, since it uses previous states to determine the next state. System allows verification of all the internal nodes with respect to the simulator response and if any mismatch, allows the user to mask unwanted data or to set the test window correctly.

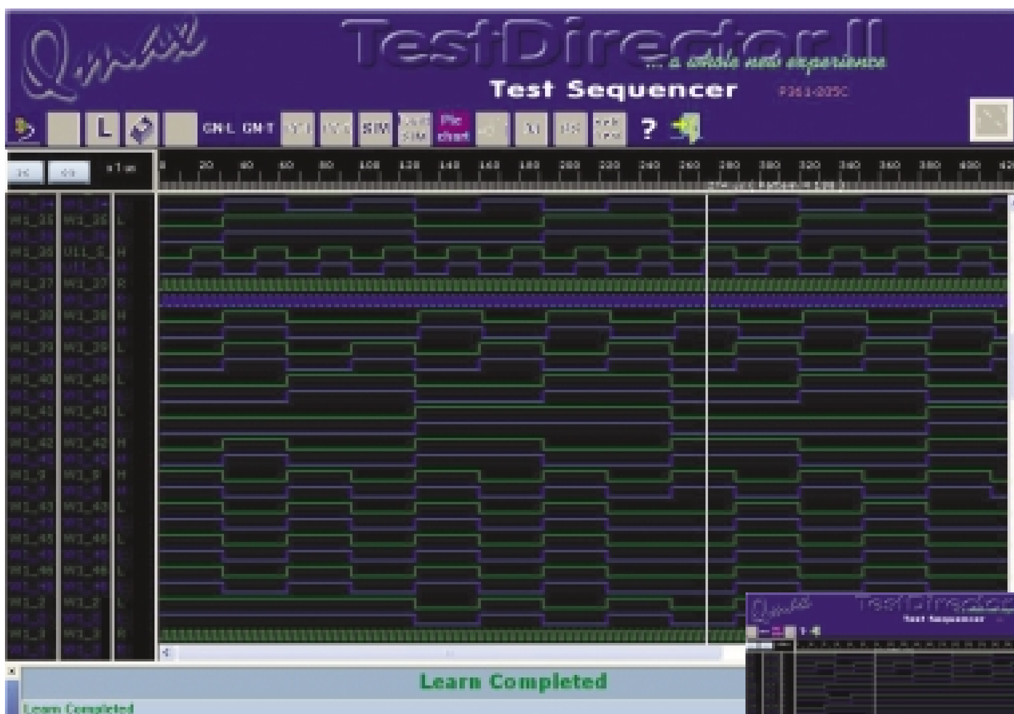
Paperless WorkStation:



While back tracking, the TD2 software can show the schematic view or the Board Layout or the Waveform window or the Back Track Tree for easy probing and diagnosing the fault as thus providing a paper less workstation,



Functional Test by Learn and Compare

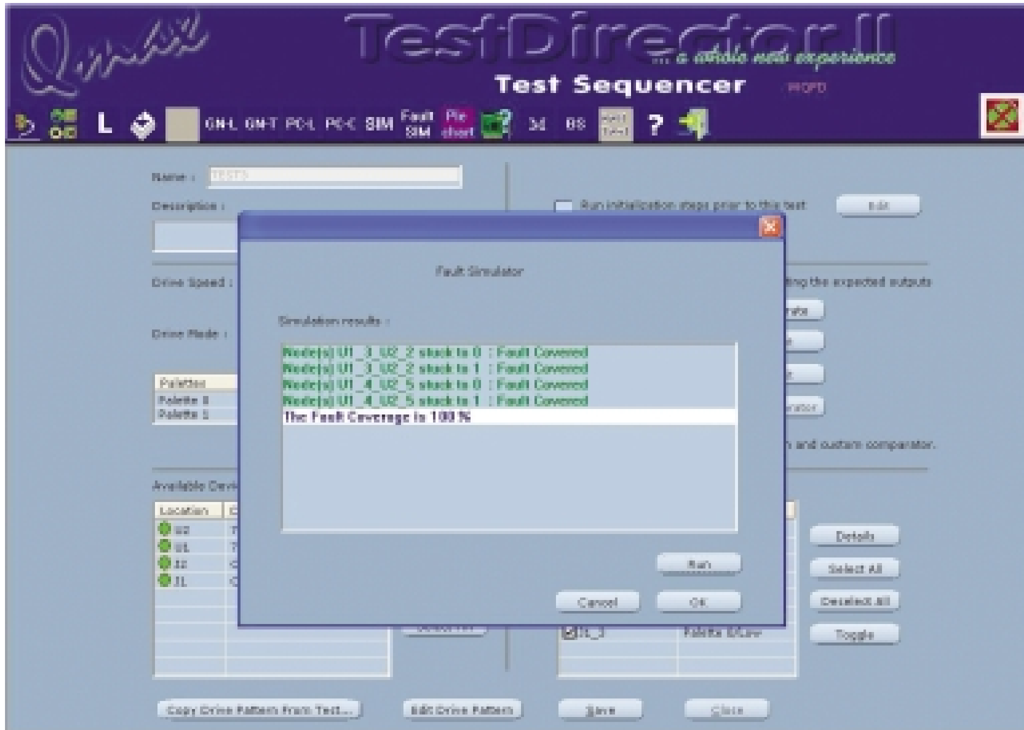


This method applies, when users cannot generate behavioral description of devices on board using VHDL. Users enter the Board NetList and generate the input sequence to initialize the board to a known state. Then for every subsequent test, user can learn the output response of the board through card edge connector and probes for internal nodes. The learnt outputs are stored in the Master Board Database for comparison in faulty boards. Users must ensure the board is initialized before learning output response and that the output response is repeatable. Net List information is used in guided probe back tracking to the origin of fault.

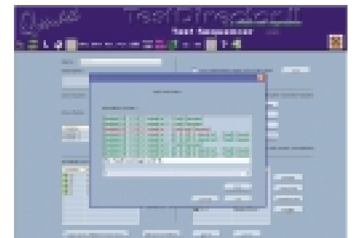
Functional Test by Combination of Simulation & Learnt method

When devices on board cannot be modeled for behavioral description, it is possible to label them as black boxes and learn their response at their outputs and pass the learnt value in place of simulated value for further simulation of other devices / nodes.

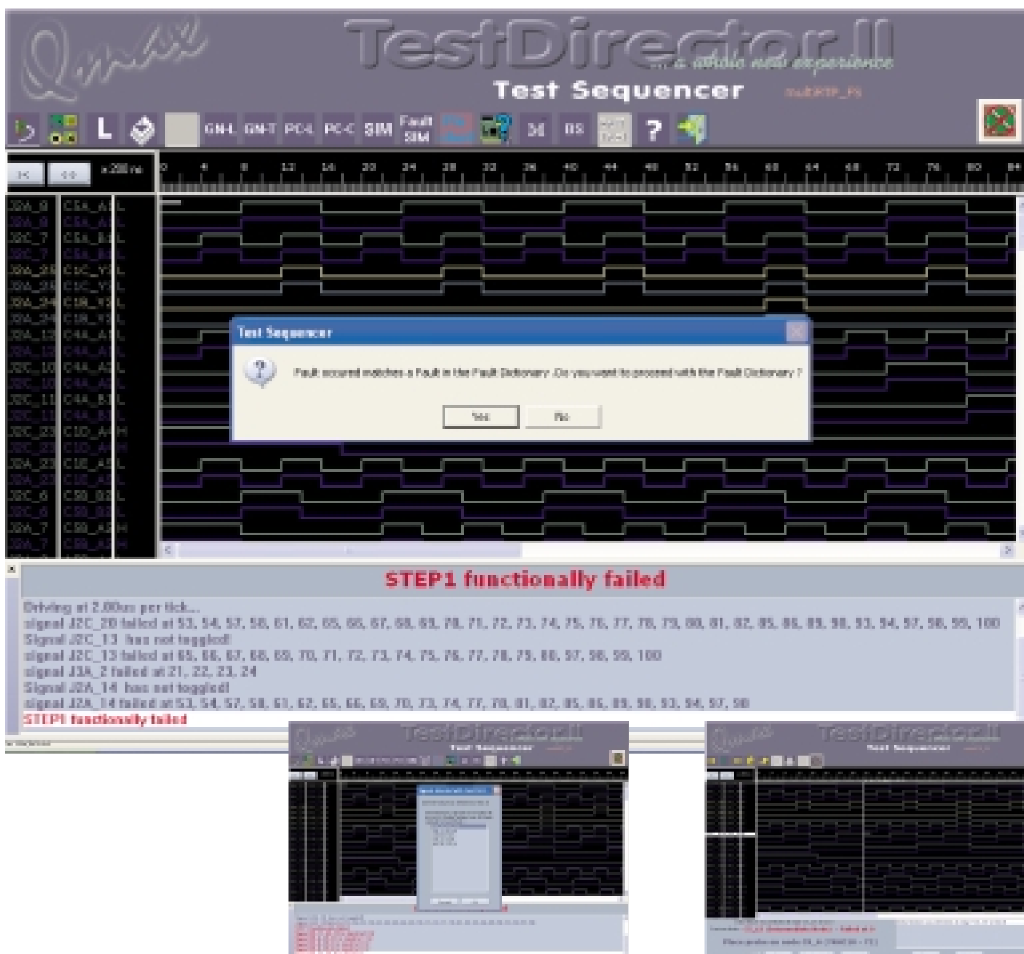
Fault Simulation *(Optional)*



While using QDDL or VHDL Simulator, Fault Simulator automatically inserts stuck-at-zero (0), stuck-at-one (1) and open (Z) faults in every node in a board and checks that the test program is capable of detecting them. If the test program covers all the simulated faults, then the confidence is stated as 100%. This helps the ATE Manager to evaluate the test programs before they are put in use. In Learn and Compare technique, insertion of faults and their detection has to be performed manually.

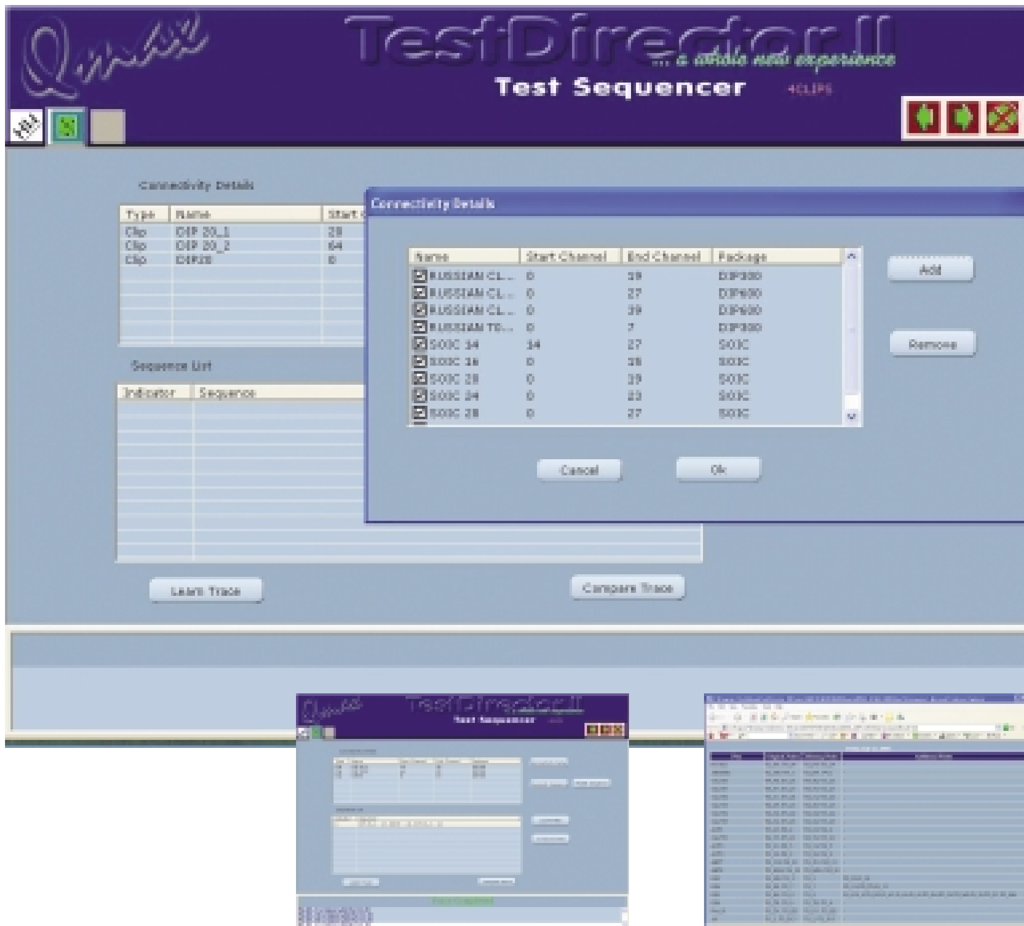


Fault Dictionary *(Optional)*



Though one can troubleshoot a Board using Functional Test and Guided Probe back tracking, the result depends on accuracy of the operator in placing the probe on the right nodes. Operator error may lead to incorrect diagnosis. Also in High density Boards it may be difficult to probe certain nodes and conformal coating may make it more difficult. At times it may not be possible to probe parts of a board when there are daughter boards on top of the main board. Fault Dictionary provides a mean to improve diagnosis under these circumstances. By the use of Fault Simulation Software, all possible faults are considered and the resulting output CRC are learnt virtually. By looking at the CRC code of failure, the system software is able to suggest probable failing components without having to probe all or if not none. Thus Fault Dictionary greatly minimizes manual probing.

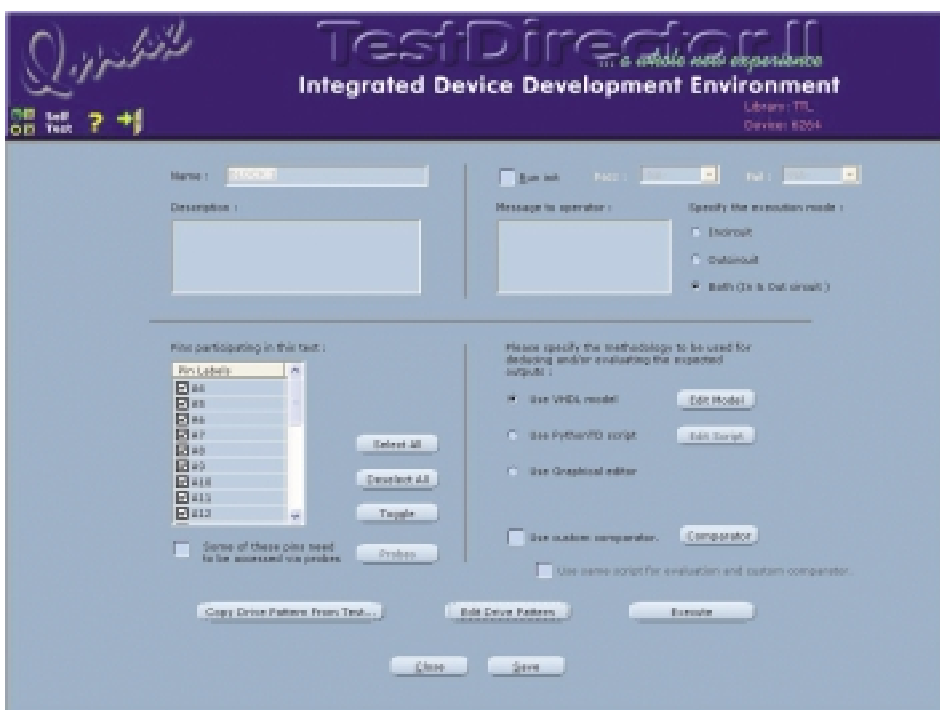
Reverse Engineering *(Optional)*

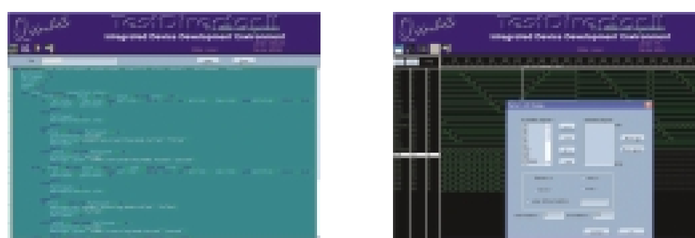


All the available Digital channels (Upto 320) can be used for Reverse engineering (CircuitTracing and Schematic Generation applications) by using the Qmax Circuit Tracing software and when it is used along with EDWIN software package, the user can reverse engineer the PCB by creating the schematic diagrams of the PCBs for which there are no circuit diagrams.

User can define any number of Clips / probes and the system will generate the sequence of placing the clips and probes automatically. The links between devices pins can be learnt and a net list generated. The resistance threshold for a link can be defined by the user.

TD2 – Integrated Device Development Environment (IDDE) *(Optional)*





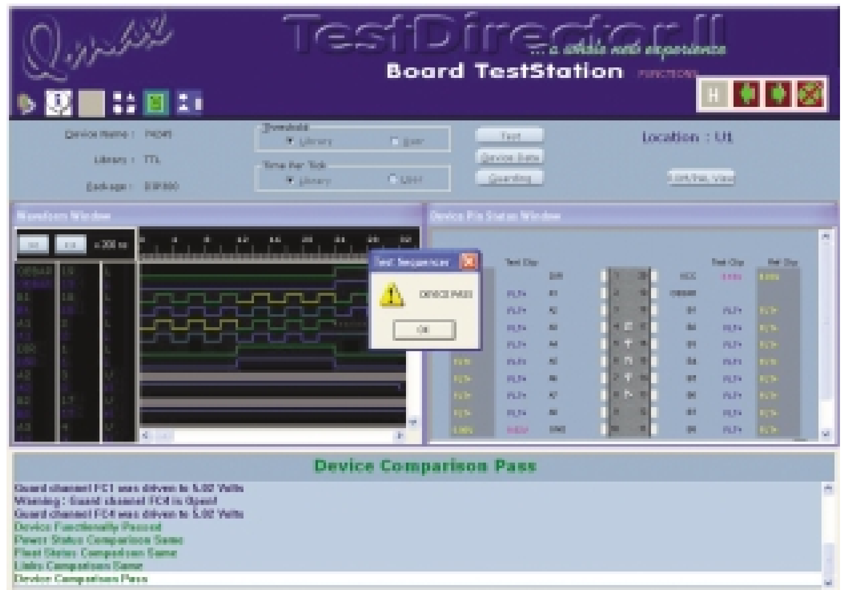
TD2 IDDE is primarily used for developing Device Level Test Programs and added to user libraries for use in TD2 Interactive, TestSequencer or TestStation.

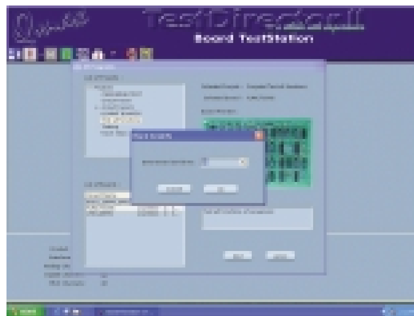
- Options of entering device packages, pin details, labels.
- Device data sheet links can be attached
- Can generate Test Vector either graphically or using PythonTD script.
- Easy generation of binary, gray pattern and user defined digital waveforms.
- Functionality of digital devices described in VHDL, an IEEE Industry standard.
- Can generate analog wave forms such as Sine, Triangle, Ramp and DC patterns.
- Expected output response can be generated using VHDL Simulator or PythonTD script or Mark for Learning / Defining methods..
- In-built / custom comparator can be used for test evaluation of analog and digital outputs.
- Facility to copy of drive patterns from the existing test programs.
- Editing of drive pattern either in graphical or in text mode possible.
- Option to Import / export device programs from one library to another is provided.

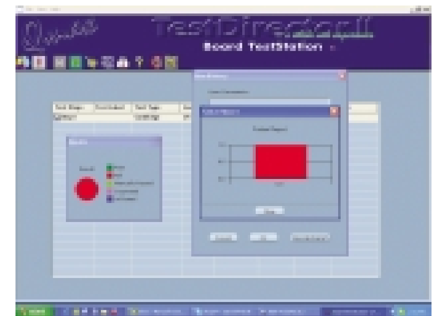
TD2 – TestStation

TD2 TestStation is operator level software with password protection along with statistical data / error log and soft operator console. Test parameters / limits can not be changed here.

- Master Board selection from database
- Enter Board under test details
- View Board repair history
- Test Board and log errors
- Clearly mark failed, suspected components
- Replace failed / suspected components.
- Test board and repeat process until the board pass.
- Create Histograms / PIE charts for MIS.
- Network capability for remote yield monitoring.
- Multi-site Test







System Hardware Specifications:

- System Controller External Pentium PC with 32 bit PCI Interface to the Test System.
- 4k x 60 bit RAM for Instruction Register and Test Sequencing. Up to 4096 test sequences can be pre-programmed to run automatically with options for conditional branching.
- The basic timing unit is programmable from 10 ns to 655µs in steps of 10ns.
- Programmable 8 Event Frames each with 8 Event Pulses for Data formatting and Test Window Placement.
- An event frame with a duration of 4 basic timing units results in 40ns data rate or 25MHz test rate. An event frame can have up to 256 basic timing units.
- Data formatting capability for NR, RO, RZ, ZD and SBC are supported.
- Four Digital highways for routing external clock, frequency measurement, time measurement between two events of UUT pins etc.
- Frequency measurements through each pin receiver with programmable thresholds up to 25 MHz. Frequency Measurements up to 50MHz through direct front panel socket.
- Pulse width measurement up to 10ns resolution, time measurement between events on any two test channels.
- External event synchronization, conditional / unconditional loop iterations of up to 64,000 loops.
- Digital measurement modes – Leading edge, Trailing edge, Dual edge, Window, Glitch and Signature Analysis mode.
- Virginia Panel Test adapter Interface for reliable UUT interface provides up to 384 signal pins, 19 Power and 19 RF connectors. 16 Bit Fixture code read for automatic recognition of Board Under Teat and loading of relevant TPS.
- Test Jig Adapters for system self-test, calibration.
- PXI Instrumentation with up to 18 slots.
- In-Circuit Measurement unit capable of measuring R, L and C values through analog highways to any test pin or probes or flying channels.
- UUT Power Supply:

  Fixed +5V @ 26A max; –5V @ 26A max:
  +12V @ 10A max; –12V @ 10A max;
  +3.3V @ 26A max

  Programmable: Up to 60V @ 12.5A max
- Maximum of 5 programmable power supplies can be installed.
- Optional Foot switch for hands free operation.

Digital Sub-System:

General configuration is 64 channel high current force driving pin drivers and 192 normal 50 ohms drivers to make up to 256 test channels. Each digital card has 32 channels. Maximum 320 digital channels can be configured in steps of 32 channel per cards.

Pin Driver / Sensor modules:

		50 Ohms Pin Driver / Sensor modules (+8, -3V)	**Force Driving Pin Driver / Sensor (+/-10V)**
Maximum Skew at Front Panel:		+/- 5ns	+/- 10ns
Driver Source impedance		50 Ohms +/-5%	8 Ohms +/-10%
Slew Rate:		600V / microsecs.	200V / microsecs.
Source Current	static:	85mA	400mA
	dynamic:	100mA	650mA
Sink Current	static:	85mA	400mA
	dynamic:	100mA	650mA
Comparator Loading		---------------- DC load 1 M Ohm with 10 pF ----------------	
Optional Programmable load current in the range of		+/-35mA.	+/-50mA.

Analog Sub-System:

System supports up to four analog channels at 20 MHz sampling speed. These can be used for Mixed Signal and analog Test, used as PMUs or used in In-Circuit Measurement of R,L,C values.

1) **As Analog Channels for Testing Analog / Mixed Signal Devices:**

   Four Independent Analog channels can be multiplexed to any of the 320 Test Channels + 8 Flying Channels.

Drive Pattern memory (Analog)	12 X 1M per Pin
Receive memory (Analog)	12 X 1M per pin
VOLTAGE / CURRENT	In 3 ranges up to +/- 13 V and +/- 260 mA
Programmable source impedances	10E, 100E, 1k, 10k, 100k, 1M and open

2) **As PMU (Precision Measurement Unit) :**

   Number of PMUs: Four multiplexed to any of the 320 channels using ultra fast reed relay.

   Force Voltage — Measure Current mode with 6 ranges.
   Capable of forcing voltage from +/-13V and current measure from +/-100mA to +/-130 nA.

   Force Current — Measure Voltage mode with 6 ranges.
   Capable of forcing current from +/-100 mA with voltage measure compliance of +/-10V.

3) **As QSM VI channels:**
   - Fully user programmable VI trace drive patterns.
   - Frequency from DC to 100KHz
   - Source impedance from 10 ohms to 1 Meg ohm.
   - Voltage range from 0.6V to 13V.
   - Drive pattern length is user programmable up to 1 Meg samples.

4) **As RLCV Measurement unit:**
   - Measure Voltage Range: +/-13V,
   - Measure Resistance Range: 10 ohms to 4 Meg Ohm,
   - Measure Capacitance: 10pF to 10,000µF,
   - Measure Inductance from 10µH to 10H.

Boundary Scan Controller:

- Basic single chain. Can be upgraded to 2 or 4 chains.
- Programmable clock frequency up to 50MHz. 128k bits RAM based drive / Sense.
- Boundary Scan operation fully synchronized with Digital / Analog pin drivers.

Bus Cycle Signature System:

- 32 bit digital signatures on every digital pin simultaneous sampling
- Signature strobe 2, Programmable bus cycle counter from 1 bus cycle to 1 Meg bus cycles.
- Reset signal polarity control.
- General / Data signatures. First bus cycle signature, First Transition signature and Bus cycle count. Signature at max bus cycle count.
- User defined logic on POD for CPU Interface.

Analog Highway Option:

- Each Analog highway card handles 32 X 12 relay matrix.
- 32 test channels from Board Under Test to 12 wire Instrument Terminal at Front Panel of the ATE system.
- These 12 wires can be either 12 single wire or Six 2 wire measurement or Three 4 wire measurement
- System can be configured up to 10 such cards or 320 X 12 relay matrix.
- Signal frequency is from DC to 30MHz.
- Voltage within +/-100V DC and current carrying capacity up to 0.5 amps.

External Instrumentation:

- Optional External Instruments such as PXI / GPIB can be installed in the system for measurements.
- PXI based 8 Slot or 18 Slot card cage can be fitted with user selected Instruments. PXI rack comes with MXI 4 interface card and copper cable.

  Choice of instrument modules include :

  - Digital Multi-meters up to 7½ digit resolution
  - Dynamic Signal Analysers
  - Arbitrary Waveform Generators
  - High Speed Digitising Oscilloscopes
  - Function Generators / Frequency Counters
  - RF Instruments like Signal Generators, RF Analysers, etc.
- System can also be configured with GPIB interface to handle many GPIB Instruments stacked in the right side rack.

System Specifications:

System Dimensions :	ATE Panel	- 1200 (H) X 800mm (W) X 800mm (D).
	Auxiliary Panel	- 1200 (H) X 600mm (W) X 800mm (D).
	External Controller Panel	- 600 (H) X 600mm (W) X 800mm (D).
System Weight :	ATE Panel	- 125 Kgs (approx. Varies with the configuration).
	Auxiliary Panel	- 84 Kgs (approx. Varies with the configuration).
	External Controller Panel	- 45 Kgs (approx. Varies with the configuration).
System Power :	110V 60Hz / 230V 50Hz	3KVA
System Operating Temperature :	25°C ±3°C	

Qmax reserves the right to change the system specifications without prior notice.
Qmax is the registered trade marks of Qmax Test Equipments Pvt Ltd. QSM is the innovative VI signature method developed by Qmax.
Windows is the registered trade mark of Microsoft Corporation. Other trade marks used in this catalogue are acknowledged.

– where standards are set; not matched

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