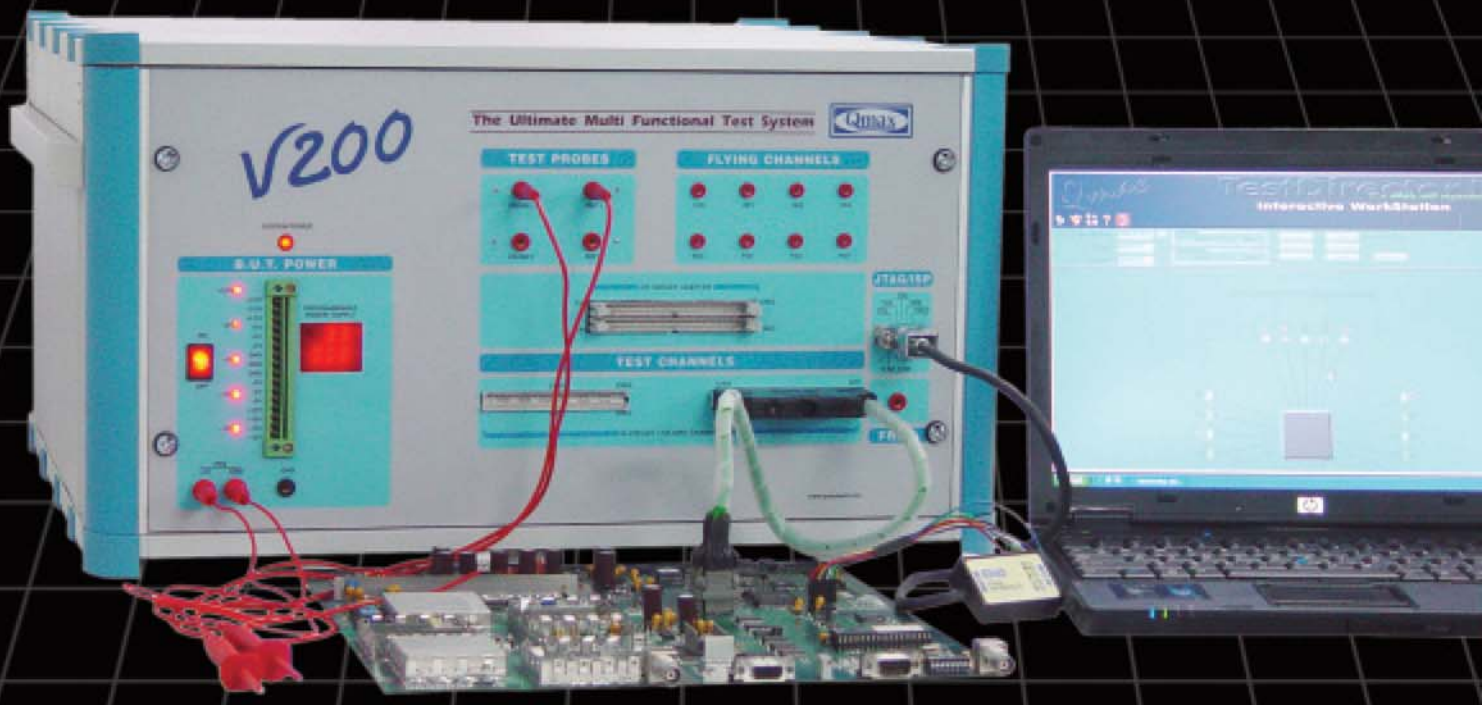
Qmax

V200

DESK-TOP ATE



Unique Features

- VHDL based Device Library
- Card Edge Functional Test
- Guided Probe back-tracking
- Integrated Boundary Scan Controller
- Fault Simulation
- Fault Dictionary
- Programmable Time base in 2000 steps
- User defined analog stimulus QSM VI
- PythonTD Test language

Qmax

Qmax V200, a tester for past, present & future PCBs / Devices and Modules

V200 is a cost effective mini ATE system, designed to cater the needs of PCB test and repair depots, keeping in mind the changing PCB technology and the challenges in testing them off-line. It can provide complete PCB test and diagnostic functions for any kind of PCB including the latest very high density complex PCBs with high pin count PQFP, FPGA VLSI chips.

It is a Combinational – Mixed Signal Test System with the addition of Boundary Scan Test for the latest generation chips. It has Card Edge Functional Test for both digital and analog, and In-Circuit Functional Test for localized test of individual devices including LSI /VLSI / Memory and Microprocessors. It also incorporates an advanced QSM VI with user definable wave pattern.

Features of V200 Hardware:

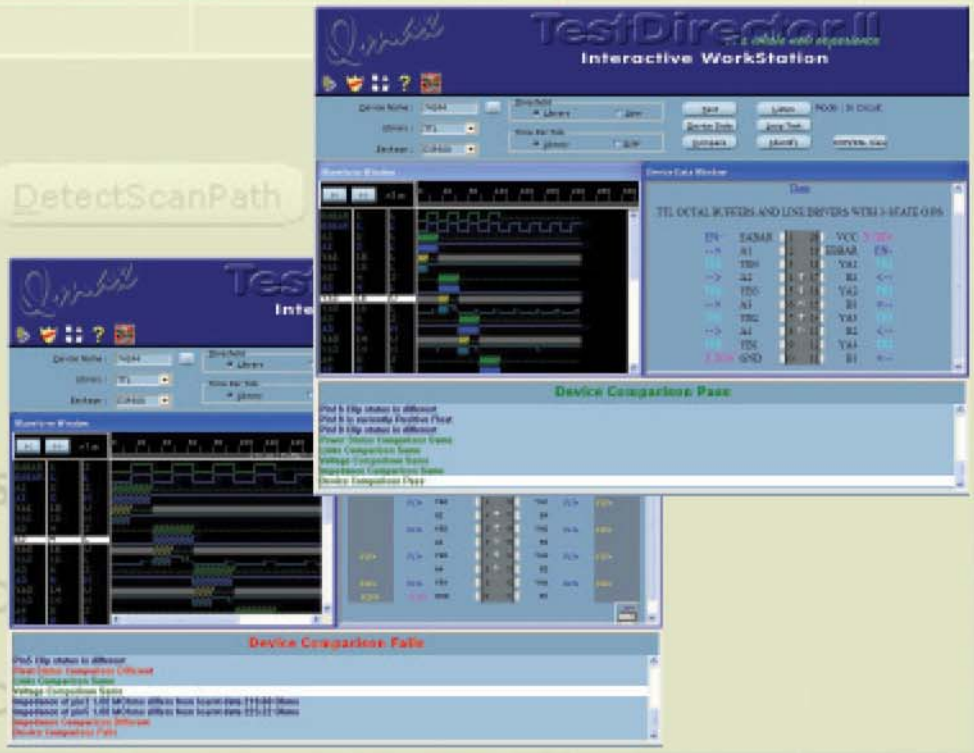
V200 is designed as a Combinational Tester with Digital /Analog and Mixed Signal Test capabilities through simple clips and probes or through card edge or as a cluster tester with a special test fixture for up to 256 test pins. In addition, it has the Boundary Scan Test option for virtual pin test where the number of virtual test pins has no physical limit. Its basic timing unit is 100ns and thus can generate test patterns at 10 MHz data rate. The timing units are programmable in 2000 steps from 100ns to 200µs, (100ns, 200ns, 300ns etc up to 200 µs) thus allowing accurate pattern timings. It has 8K x 4 RAM behind each digital pin electronics and 8K x 24 RAM behind every analog channel. Its advanced sequencer allows external event synchronization or handshake, which are very essential in complex microprocessor tests.

TestDirector II ... a whole new experience

TD2 Interactive WorkStation

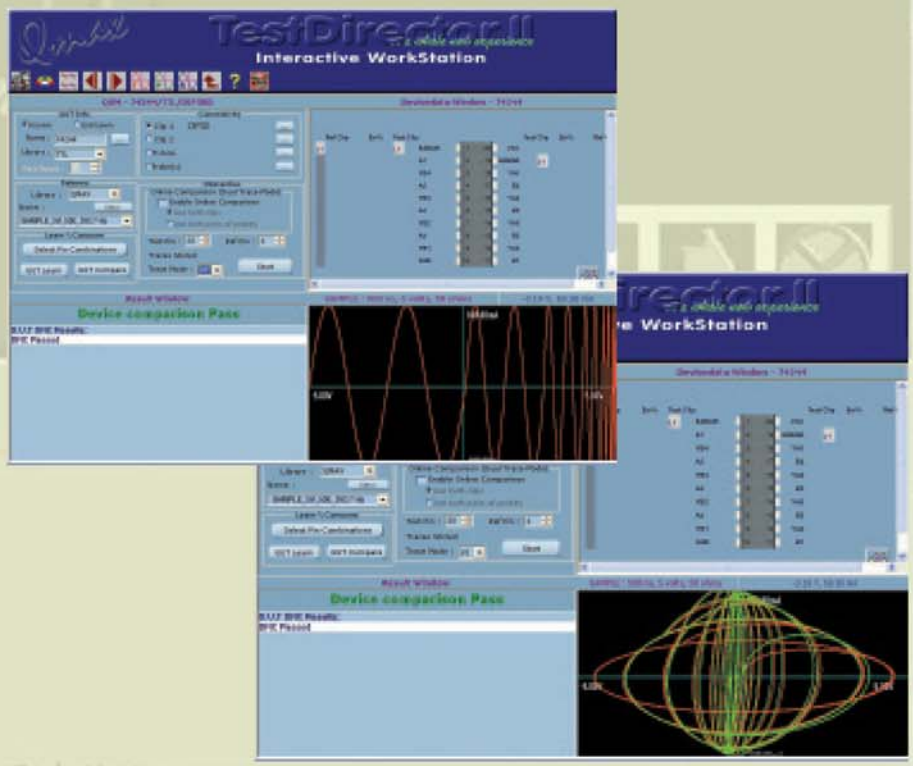
In-Circuit Functional Test at its Best

- Functional Test facility for testing individual ICs in In-Circuit or Out-of-Circuit.
- Pin Status Check & In-built DRC (Design Rule Checker).
- IEEE Standard VHDL language in behavioral description of the function of the chip in its library.
- PythonTD Test language for Analog / Mixed signal device stimulus and output evaluation.
- Auto compensation is extended for all digital devices (not limiting to SSI /MSI) and thus LSI / VLSI chips can be tested in its In-Circuit configuration without the need to learn from a known good board.
- Unified Library of 31K+ devices and device test comprehensives report for validation of Library Test programs developed by a user.



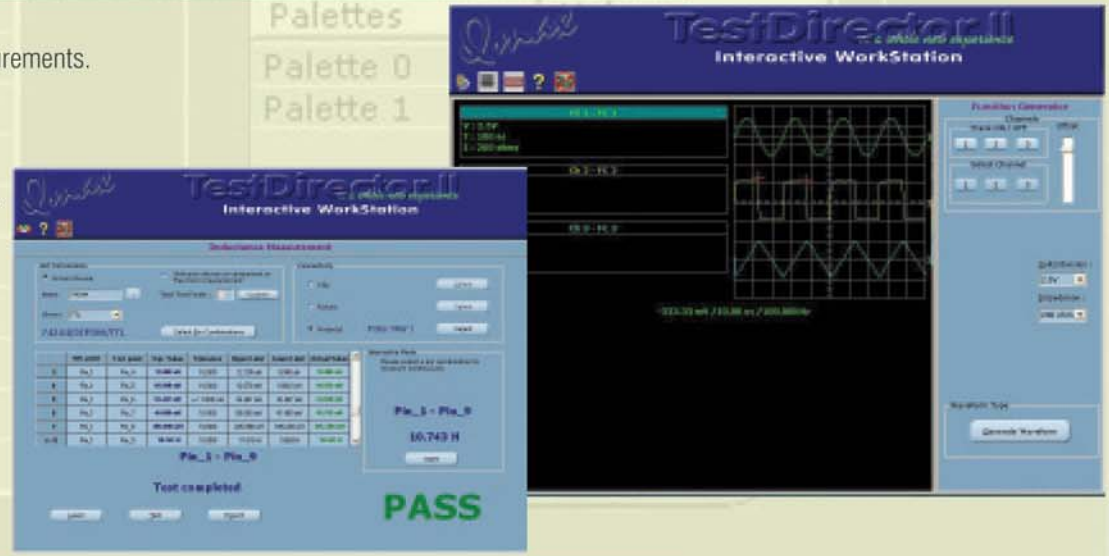
User defined QSM VI Stimulus

- User defined wave pattern as stimulus for VI Trace and thus not limiting the VI trace to simple sine wave alone.
- User defined wave pattern can be any mathematical wave shape such as sine / triangle /square /step /ramp or even arbitrary patterns as desired by user and can be stored in the Library for possible re-use.
- The frequency is fully programmable from as fast as 100 KHz down to 1 Hz as a result of *V200*'s vast time base selection capability.
- Programmable amplitude, source impedance.
- Use of Step wave is useful in analyzing transient response of node.
- Frequecy Sweep generation to trace the frequency response of a node.
- Incorporates interactive mode as well as learn and compare.
- Fixed Reference, any pin to any pin or user combination.



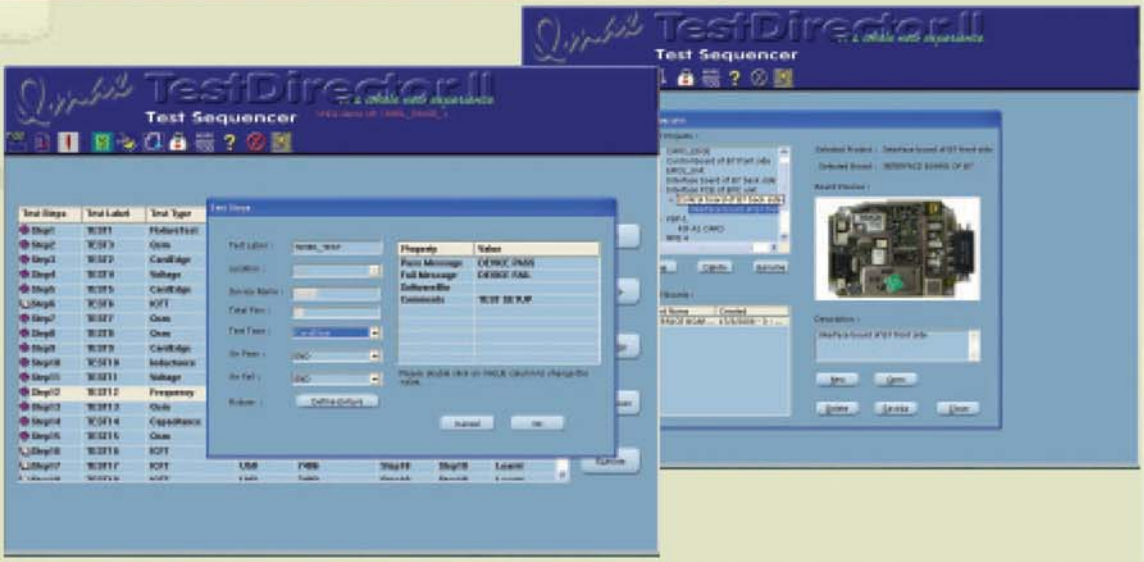
Measurement Functions & Other Utilities

- Resistance / Inductance / Capacitance / Voltage Measurements.
- Diode Measurements.
- Frequency Measurement.
- Period /Time Measurements.
- 3 Channel - 20 Mega Sample Scope with Programmable Load.
- 3 Channel Function Generator



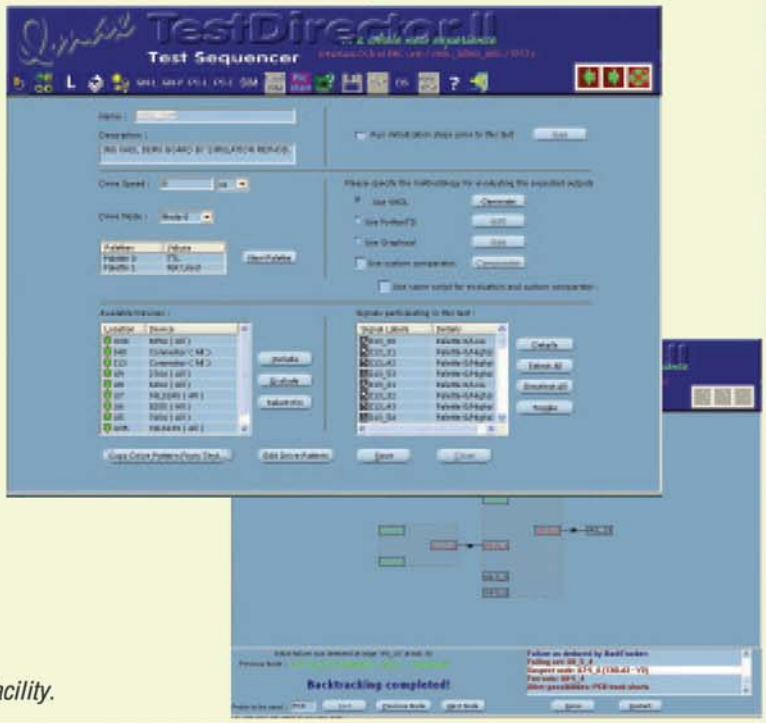
TD2 TestSequencer

- For Sequencing of multiple tests with conditional branching, messaging, user prompting, external trigger and external handshake.
- Board level test using combination of isolated device test (ICFT), QSM VI, Measurements, Card Edge Functional Test, Integrated Card Edge + Boundary Scan Test*, all in one test program.



Card Edge Functional Test at its Best

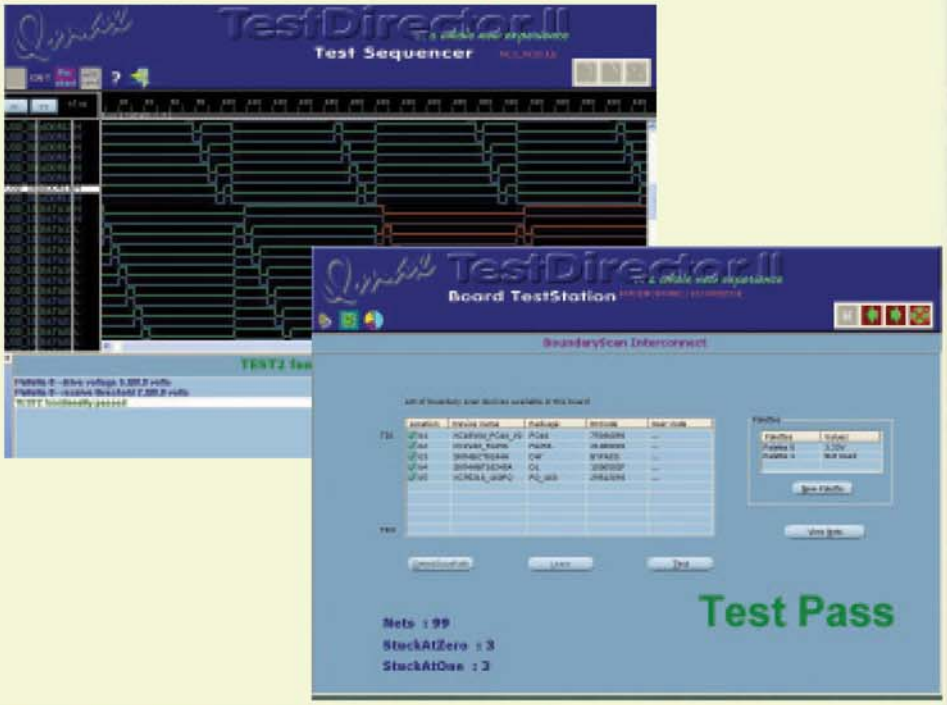
- User can develop test program for complex boards with ASICs and BGAs, where no functional data are available.
- User can generate the test vectors using the graphical waveform editor or PythonTD test vector generator, where the primary I/O pins can be either physical edge pin / In-Circuit pin or a JTAG Virtual Boundary Scan Pin.
- User can either learn from a known good board, the expected output response or define the expected using either graphical waveform editor or the PythonTD test language with mask / tolerance editing facilities.
- Graphical waveform editor and PythonTD supports Digital / Analog and Mixed Signal I/Os.
- The Test program developed can be used for a device / cluster or a complete PCB.
- In case of cluster or whole board, user needs to input the netlist of the circuit, assign input /output pins for tester channel for automatic generation of guided probe back tracking of internal nodes.



** Boundary Scan Software need to be purchased for enabling this facility.*

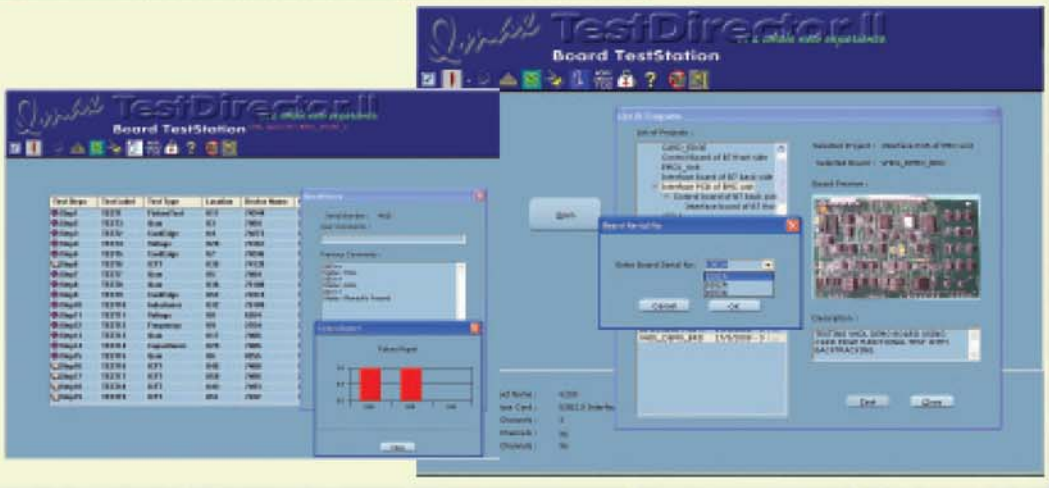
Boundary Scan Test Software *(Optional)*

- Boundary Scan uses simple 5-wire connector (J-TAG) to interface to the PCB under test, eliminating the need for test pin contact (Virtual Test Pin Test Concept).
- Using Boundary Scan Software package and vendor supplied BSD Files, ID Code Read, User Code Read, Integrity Test and Interconnect Test can be performed.
- Learn and compare option for interconnect test, where no netlist is available.
- Functional Test for BS devices and Non-Boundary Scan Devices (Glue Logic Chips).
- Integrated Card Edge and Boundary Scan Test for Interconnect Test and Board Functional Test.



TD2 TestStation

- Programs developed in TestDirector II TestSequencer can be exported to TestStation
- Test only usage and no program /data /tolerance can be modified.
- For operator use only.
- User defined Error Log reporting, Failure analysis, statistics and data log.
- Optional Remote Monitoring of yield and statistics.

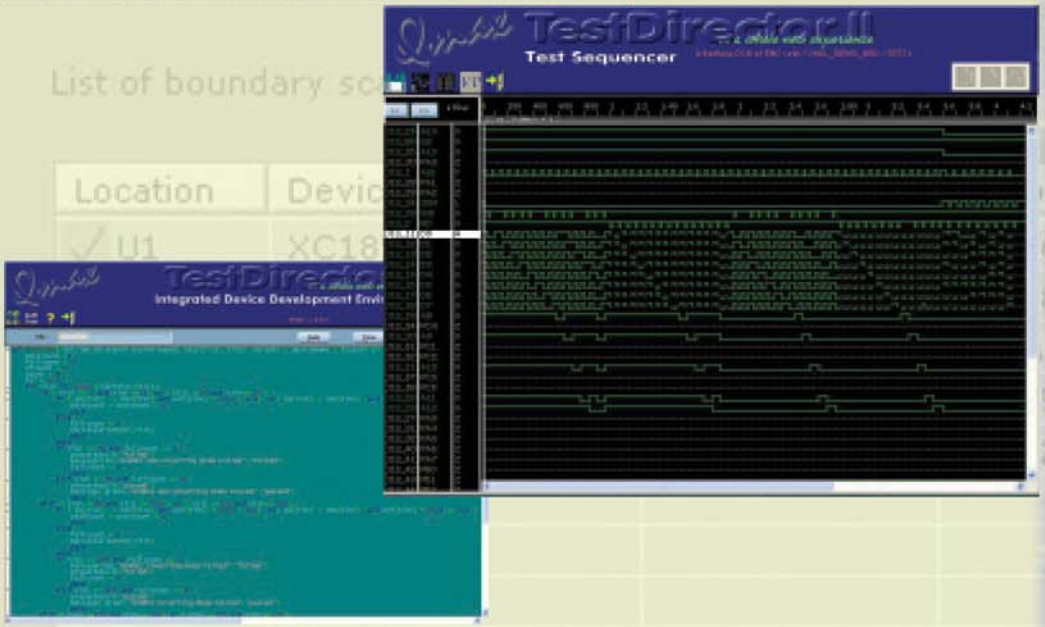


TD2 IDDE *(Optional)*

- For developing new Digital Device Models in the library using VHDL functional behavior.
- For developing new Analog / Mixed signal device models using PythonTD Test Language and adding it in the Library.
- Graphical Test Program Generation feature

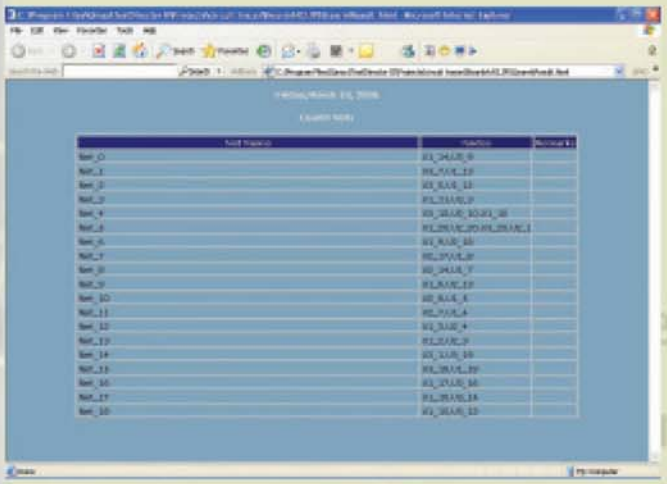
TD2 TestSim Suite *(Optional)*

- For Board Level VHDL model creation and functional simulation of the board using VHDL. Advanced On-Line Simulation support for increased fault coverage for boards that fail to initialize.
- Automatic Guided Probe Back Tracking for Fault Isolation up to node level.
- Fault Simulation Software for Board Test Program validation and test comprehensiveness.
- Fault Dictionary Software for nil or minimized internal node probing.



TD2 CircuitTracer *(Optional)*

- Using multiple clips, Edge connectors / Probes and JTAG IO pins, the connectivity between devices can be learnt and a netlist created.
- Created net list can be imported into optional Edwin CAD package for schematic generation.



SPECIFICATIONS

SYSTEM

Test Points	Up to 96 Digital In-Circuit Testing (16 Ch. per card) Up to 256 Analog Signature Testing Un-limited Virtual Test Points
Pattern Rate	10 MHz -Digital testing (Max.), 10 MHz -Analog testing, (20 MHz sampling rate) 100 KHz – QSM VI
Time Base	Programmable from 100ns to 200µs in steps of 100ns (2000 steps)
Dynamic Guarding	Up to 8 channels, allocated automatically

DRIVERS / SENSORS

DIGITAL

Driver/Sensor card	16 ch.bi-directional RAM based ch. per card up to 96 max
Drive Level & Resolution	±10V programmable in 80 mV steps
Sense Level & Resolution	±10V programmable in 40 mV steps
Current	650 mA sink & source limit
Driver state	Hi, Low and Tri-state

ANALOG

No. of Channels	Three, each 12 bit DAC / ADC RAM based,
Analog Multiplexer	Switchable to any test channel available.
Driver output current	250mA per pin /ch.
Drive Pattern	User definable and standard waveform
Drive Source Impedance	Programmable in 5 steps
Drive current/voltage	± 250mA maximum / ±13 volt per Channel.
Measurment	R- upto 1M, C- upto 10,000µF, L- upto 10 H, V- upto 13V and F- upto 50 MHz.

IN-CIRCUIT TEST

Digital	Clip on test using systems device library and simulator output.
Analog	Clip on test using systems device library and simulator/ calculated output.
SIMULATOR	Industry grade VHDL simulator

DIGITAL OSCILLOSCOPE

No. of channel	minimum 3 (signal or multiple trace)
Resolution	12 bit
Amplitude	0-13 V (in 5 range)
Time base	80 µ sec. to 9.6 milli sec.
Trigger	Auto, Normal, Signal, Positive or Negative
Impedance	50 Ohm to 5 M.Ohm
Memory	8K memory per channel

POWER SUPPLY

Fixed Power Supply	Built-in +12V@13 amps. -12V@13 amps, +5V@25 amps, -5V@25 amps. and 3.3V@25 amps

V-I CURVE TRACING

No. of Channels	96 expandable up to 128 Channels
Test Voltage	2.5V to 12V peak to peak
Source Impedance	Programmable from 200 Ohms to l000 Kohms
Waveform mode	VI, VT, VZ
Test frequency	Smooth selection of frequency up to 100 KHz.
VI Curve Tracing	Available for discrete components like DIP, SOIC, PLCC, QFP, PQFP, Transistor, Diodes etc…
Curve Comparison	Capable of comparing different curves and diagnose the faulty curves.
Curve Storage Facility	Available.
Analog ICs	Features for testing of analog devices such as OP-Amps, Regulators, Comparators and ADCs/ DACs. Opto-couplers, Transistors, SCRs/FETs, DIACs/TRIACS, Switches and Special functions analog ICs including SMT devices.
Programmable Load Resistance	50 Ohms to 1000 K Ohms
Device data sheets	Available for the devices in the library

OTHER FEATURES

Size of test	8K-deep test vectors in single burst mode. Unlimited vector depth in interactive hand shake mode.
ESD test	0.065mA min @13V to 25mA max@2.5V at 2.5 KHz. Max.
Dual Signature trace	Standard feature. Signature plotting through two probes or set of Clips.
On board Clock disable H/W	Disable clock disturbance while testing In-circuit.

TEST SOFTWARE

TD2 Interactive WorkStation	Standard.
TD2 TestSequencer	Standard.
TD2 TestStation	Standard
TD2 TestSim Suite	Optional
CircuitTracer for Reverse engineering	Optional
Edwin for Windows XP for schematic generation	Optional
Boundary Scanning S/W	Optional

GENERAL *(Recommended)*

Controller	Pentium IV PC
Operating System	Windows XP Professional SP2
RAM	Minimum 1 GB
Hard Disk	80 GB with 2 partition
Interface	USB 2.0 (min. of 4 USB ports)
User Control	keyboard / Mouse / Optional – Foot switch / external trigger.
Test Interface	Clips – Probes / Card edge / customized test fixtures / J-TAG

TEST INTERFACE

IN-CIRCUIT WALKING CLIPS

DIP Clips –Top access	8-64 pins
DIP Clips – Bottom	8-40 pins
PLCC – Clips	up to 84 pins
SOIC – Clips	up to 28 pins
QFP – Clips	On request
TO5 package	
TO9 package	
Russian Device Clips	up to 40 pins
JTAG	5 wire connector for boundary scan tests.

OUT – CIRCUIT

DIP 40 & 64

SMDs – SOP / TSOP / PQFP / SOIC / SOJ / PLCC up to 64 pins

CUSTOMISED

Card edge / Bed of nails

Qmax

— where standards are set; not matched.

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